UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,668	12/02/2003	Ciaran J. Brennan	END920030076US1	5075

EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2138	

23122 7590 04/03/2006

RATNERPRESTIA
P O BOX 980
VALLEY FORGE, PA 19482-0980

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/725,668	Applicant(s) BRENNAN ET AL.	
	Examiner John P. Trimmings	Art Unit 2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/02/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are presented for examination.

Information Disclosure Statement

1. The examiner has considered the Information Disclosure Statement dated 12/2/2003.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The limitation, "using the second set of timings [of Claim 8, 7] to provide a fourth stress" is not enabled by the disclosure because there is no recital pertaining to an additional stress being applied during the 2nd BIST sequence to the second timings. Since the applicant has not described the fourth stress as included with the second timings, therein being no specific enabling disclosure, the examiner cannot speculate as to the nature of the limitation. Thus the limitation is not enabled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5, 7-8 and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Giles et al. (herein Giles), U.S. Patent No. 6085334.

As per Claim 1:

Giles teaches a method of manufacturing a device having embedded memory (column 3 lines 56-58) including a plurality of memory cells (column 3 line 61), the method comprising the steps of: applying a first test stress to selected cells of the plurality of memory cells with a built-in self test; identifying at least one weak memory cell; repairing the at least one weak memory cell; and applying a second test stress to the selected cells and the repaired cells with the built-in self test (column 3 lines 58-67, column 4 lines 1-7).

As per Claim 2:

Giles further teaches the method of claim 1, wherein the step of applying a first test stress further comprises the step of operating the memory cells with a timing that exceeds an operational timing (column 8 lines 5-15).

As per Claim 3:

Giles further teaches the method of claim 1, further comprising the step of applying the first test stress in at least one of a plurality of test sequences (column 8 lines 16-24).

As per Claim 5:

Giles further teaches the method of claim 1, further comprising the step of applying the second test stress in at least one of a second plurality of test sequences (column 8 lines 37-54).

As per Claim 7:

Giles teaches a method for testing during manufacturing a device having embedded memory (column 3 lines 56-58) including a plurality of memory cells (column 3 line 61), the method comprising the steps of: applying a first set of timings to selected cells of the plurality of memory cells using built-in self test controls (column 8 lines 5-15); testing the selected cells using the first set of timings (FIG.5 72); identifying weak memory cells (column 5 lines 16-37); repairing the weak memory cells (column 8 lines 16-20); applying a second set of timings to the selected cells and the repaired cells using the built-in self test controls (FIG.5 78); and testing the selected cells and the repaired cells using the second set of timings (FIG.5 80).

As per Claim 8:

Giles further teaches the method of claim 7, wherein the first set of timings provides at least a first stress to the cells and the second set of timings provides at least a second stress to the cells (column 8 lines 5-50).

As per Claim 11:

Giles further teaches the method of claim 8, further comprising the steps of using the first set of timings to provide at least a third stress to the cells (column 8 lines 37-40) and using the second set of timings to provide at least a fourth stress to the cells (the multiple condition feature of column 8 lines 37-40 encompasses timing (frequency) and other conditions such as voltage or temperature).

As per Claim 12:

Giles teaches a method of manufacturing a device having embedded memory (column 3 lines 56-58) including a plurality of memory cells (column 3 line 61), the method comprising the steps of: (a) providing a first plurality of timings and a second plurality of timings to built-in self test controls (column 8 lines 5-15); (b) applying at least one of the first plurality of timings to selected cells using the built-in self test controls (column 8 lines 16-24); (c) identifying failed memory cells (column 8 lines 25-30); (d) repairing the failed memory cells (column 8 lines 25-30); and (e) repeating steps (b) to (d) by applying additional selected ones of the first plurality of timings to the cells (column 8 lines 20-23).

As per Claim 13:

Giles further teaches the method of claim 12 further comprising the step of (f) applying at least one of the second plurality of timings to each of the cells using the built-in self test controls (column 8 lines 37-41).

As per Claim 14:

Giles further teaches the method of claim 13 further comprising the step of (g) repeating step (f) by applying additional selected ones of the second plurality of timings to each of the cells (column 8 lines 50-53).

4. Claims 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Templeton et al. (herein Templeton), U.S. Patent No. 6973605.

As per Claim 15:

Templeton teaches a device for testing an embedded memory (see Abstract) having a plurality of memory cells (FIG.2 206) during manufacture of the embedded memory, the device comprising: a first timer (first output of FIG.4 402) for applying a plurality of timings to the memory cells (internal clock pulses 302); a second timer (second output of FIG.4 402) for modifying at least one of the plurality of timings (stress clock pulses 304); and a logic circuit (FIG.2 BIST 204) for testing the memory cells by applying the at least one of the plurality of timings to the memory cells (using FIG.4 410 Stress Test Select).

As per Claim 16:

Templeton further teaches the device of claim 15, further comprising a sensor coupled to the memory cells (FIG.2 BIST 204) for determining whether the memory cells failed the testing (column 6 lines 61-67); and a repair component for repairing failed cells (FIG.2 202 BISR and 208 Redundancy Control).

As per Claim 17:

Templeton further teaches the device of claim 15, wherein the first timer (FIG.4 302) includes the second timer (FIG.4 304) and the second timer includes a delay circuit (minus margin of FIG.3 t_{314}), for modifying the at least one of the plurality of timings (FIG.3 Stress CLK 304).

As per Claim 18:

Templeton further teaches the device of claim 17, wherein the first and second timers are located in at least one area of the embedded memory (see Abstract).

As per Claim 19:

Templeton further teaches the device of claim 15, wherein the embedded memory includes a built-in self test for controlling the testing for determining whether any memory cells failed the testing (FIG.2 204).

As per Claim 20:

Templeton further teaches the device of claim 19, wherein the embedded memory includes a built-in self repair for repairing failed memory cells (FIG.2 202).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4, 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giles et al. (herein Giles), U.S. Patent No. 6085334 as applied to claims 1 and 8 above, and further in view of Templeton et al. (herein Templeton), U.S. Patent No. 6973605.

As per Claim 6:

Giles fails to further disclose the method of claim 1, wherein the step of applying a first test stress includes the step of operating each memory cell with at least one tight timing, the at least one tight timing being shorter than an operational timing. But such a feature is disclosed in Templeton in FIG.3 Timing Chart for the Stress CLK signal 304, which is based on a shortened version of the operational clock 210. Templeton, in column 4 lines 12-32, cites the advantage being a self-test/self-repair process that detects and repairs weak memory cells under more stressful conditions not found during normal memory operation. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include the memory timing stress system of Templeton in the Giles system in order to detect marginal and weak memory cells not otherwise detected.

As per Claims 4 and 9:

Giles fails to further disclose the method of claims 1 and 8, wherein the second set of timings tests the memory cells at an operational timing. Templeton, in FIG.5, suggests that, following repair of cells under stress conditions, that step 512 be executed where the clock is set back to the normal operating range (column 9 lines 4-15). And in view of the motivation previously stated, the claims are rejected.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giles et al. (herein Giles), U.S. Patent No. 6085334. Giles discloses the method of claim 8, wherein the first set of timings tests the memory cells at timings that are faster than an operational timing. Giles states that the first stress factors may be frequency (column 8 lines 5-15). One with ordinary skill in the art at the time of the invention, motivated to self-testing a memory relative to environmental conditions (column 2 lines 27-40) would have found it obvious to use frequency variations, and one of which would obviously be a higher clock frequency. Use of faster timing through frequency variations would have been obvious in order to detect errors under varying environmental conditions, and so the claim is rejected as being obvious over Giles.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2138

jpt

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100